Open access Journal International Journal of Emerging Trends in Science and Technology

A Novel Approach FPGA Based High Performance Wireless Embedded System

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Abstract
Traditional wired system has limited performance and complex system with low sample rate for multiple applications. For particular application it needs to design particular hardware and software. With wireless system low-power modules that offer limited computational performance and communication bandwidth .In this paper, A hardware platform which combines microcontroller and FPGA is presented. This platform has features that allow easy reuse of the hardware in several applications avoiding redesigning the system. The flexibility provided through dynamically configurable interfaces and power management, helps optimizing performance and power consumption for different applications.
Keywords: *FPGA, Microcontroller, wireless system low power.*

1. Introduction

The limited bandwidth and high-power consumption of radio transceivers that are typically used, the major challenge lies in transmitting a large amount of data generated by high-sample rate applications. In order to overcome this challenge, researchers have proposed in-sensor processing in which, raw data is processed locally in a sensor node, and only results are transmitted wirelessly. Therefore, it reduces communication activity and the associated power consumption.

However, it is observed that typical low-power micro- controllers integrated in sensor nodes, often lack high-throughput performance when complex mathematical and signal processing algorithms are involved. Therefore, to meet the demands of high computational performance, the prototype design reported in employs a high throughput micro-controller.for in-sensor data processing, in addition to a low-power 8-bit micro-controller.

FPGA-based commercial evaluation kits and micro-controller based wireless nodes were used to investigate their performance and energy consumption for high-sample rate applications.

Based on the presented results in these articles, it can be concluded that high-throughput processing requirements can only be fulfilled through an FPGA, however, by accurately distributing the processing, communication and control specific tasks on a micro-controller and an FPGA, it is possible to optimize both the performance and power consumption for an application.

Apart from that, inter module communication interfaces such as between FPGA and micro-controller, and between wireless transceiver and micro-controller are fixed in these nodes and therefore, cannot be re- Configured for different applications without modifying the hardware design. Additionally, the compactness of these nodes is compromised because of the extra height, resulting from the interface connectors on both sides of a layer and also stacking of four layers on top of each other to form a complete working node.

2. Hardware

A simplified design of platform, representing all major components and their interconnections is shown in Figure 1. With the exception of power

source, all other components are integrated in the platform.

2.1 block diagram

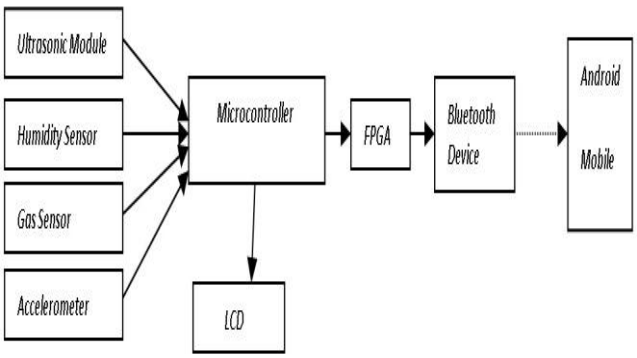

Figure 1: Block diagram

In order to achieve a high-computational performance, two processing resources, a PIC micro-controller PIC16f877A and a Spartan-6 FPGA XC35250 are integrated together.

2.2 Hardware description

The micro-controller can be used to process the application data, read the sensor's data, and/or communicate with the radio transceiver in order to transmit or receive data/results. In addition to its application dependent data processing, the micro-controller performs all the control specific operations such as power and FPGA configuration management and therefore, acts as a central control unit in the platform. The micro-controller can be used as the main processing unit for a wide variety of monitoring applications

In order to achieve a high-throughput computational performance as required in many high-sample rate applications, the FPGA is integrated into the platform. Due to hardware parallelism, it is possible for multiple independent tasks to be realized using dedicated hardware logic in the FPGA, which thus be performed simultaneously at high speed..In addition, the re-configurability of the FPGA allows synthesizing different algorithms with optimized control and data paths, without modifying any real hardware.

In order to enable wireless communication in the platform, an IEEE 802.15.4 compliant low-power radio transceiver, HC05(CC2540) is integrated in the design. The transceiver operates at the 2.4 GHz license free band and provides a maximum throughput of 250 kbps.

So here microcontroller reading sensors output and processing data in microcontroller and in FPGA output is displayed through radio transceiver on android mobile with use of self developed android application.

3. Software

In order to use this platform for an application, supporting software must be developed for both the micro-controller and the FPGA. Currently, this is achieved using two different software development environments

The programming is done in c code so its user friendly. For both PIC and FPGA different software is used to burn code and to write code. Arduino is used to write and burn the code in FPGA and PICKIT is used to burn the code in PIC . And mikro c used to write code for PIC. Diptrace is used for pcb designing.

4. Future scope

In addition, the dynamic power management and reconfigurable architecture can be exploited to optimize performance and power consumption according to different applications. The flexibility provided through dynamically configurable interfaces, customizable communication between the micro- controller and the FPGA, and dynamic power management can also be used to explore efficient architectures for different monitoring applications.

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Author Profile

Priyadarshani Kokate received the B.E degree in Electronics and telecommunications Engineering from Sinhgad Academy of engineering in 2013 and currently pursuing M.E in vlsi and embedded system from savitribai Phule Pune University from Pune INDIA.